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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/099,754	03/14/2002	Michael J. Peters	00939s-050510US	9162

20350 7590 05/25/2006

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EXAMINER	
SAXENA, AKASH	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 05/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/099,754	PETERS ET AL.	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,8-10 and 13-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 8-10, 13-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claim(s) 1-3, 8-10, 13-17 have been presented for examination based on amendment filed on 14th November 2005.
2. There is no amendment to the claims.
3. Previous non-final office action mailed on 14th June 2005 is incorporated within this office action unless otherwise specified where the more current rejection for the amended claims supercedes the previous rejection.
4. The arguments submitted by the applicant have been fully considered. Claims 1-3, 8-10, 13-17 remain rejected. The examiner's response is as follows.

Response to Applicant's Remarks & Examiner's Withdrawals

5. The examiner respectfully maintains the claim objection(s) to claim(s) 15 as there is no attempt by applicant to clarify the objection.
6. The examiner respectfully maintains the claim rejection(s) under 35 USC § 102 to claim(s) 1-3, 8-10 and 13-17 under the SPICE I references as applicant has not cited portion of the earlier disclosure (now US Patent 6,480,817) that is germane to the invention as claimed in the divisional application to assist examiner in assigning appropriate priority to the claims. See MPEP 201.06.

   Examiner withdraws the rejection related to the SPICE II. SPICE I teaches the limitation present (SPICE I: Pg.29 Model Card describing a model and having various levels of input and out – as analog circuit; Pg.37 Sub-circuit design allows for combination of models to design complex circuits) at least in claim 1 and dependent limitations are rejected likewise.

Response to Applicant's Remarks for 35 U.S.C. § 102

7. Claim were rejected under 35 U.S.C. 102(e) as being anticipated by Hsieh'800.

Regarding Claim 1

Applicant has argued, "simulation system of claim 1 is not a bidirectional buffer" and is "instead a system for simulating (or modeling) signals in an electronic apparatus". The examiner respectfully disagrees, as the bidirectional buffer is also an electronic circuit and represents a system for modeling a bidirectional flow like an I/O pad (Hsieh '800: Abstract Lines 1-3; Col.2, Lines 26-28; Figure 4). Hsieh '800 clearly teaches using a FPGA (used in art for modeling circuits) to design input out put interconnects (Hsieh '800: Col.1 Lines 25-37). FPGA as taught by Hsieh '800 shows a system for modeling interconnect or I/O (bidirectional) signals.

Applicant further argues, "means for" language. Applicant has neither pointed in disclosure for support for these limitations nor has stated how the prior art fails to anticipate the specifics of the claim. Applicant has merely cited *supposed presumption* made in the office action without further argument.

Applicant has further argued, "single shot device 104, however, does not generate a third value, based on the first value and a second value. Rather, it merely determines whether buffer 100 should be driven low or high". Examiner respectfully disagrees. Firstly, there is no definition provided how the third value differs from the first value and second value in the disclosure or the claim. Secondly, third value is generated based on the first value and second value as both are used to determine the action of the one shot device 104. Thirdly, there is no limitation present in the

claim as to what the third value is used for; therefore the argument that it is merely used to drive buffer 100 is an allegation. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., output too buffer from the third value) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant's argument regarding inherency are considered and are found to be unpersuasive. The limitation disclosed in claim 1 are also present in claims 2-3, 8-19 and 17 and these claims remain rejected likewise.

Response to Applicant's Remarks for 35 U.S.C. § 103

8. Claim 2 was rejected under 35 U.S.C. 103(a) as being unpatentable over Hsieh '800 in view of Huang'593.

Regarding Claim 2

Applicant has argued that Hsieh '800 and like wise Huang'593 fails to show system for simulating a bi-directional signal. Examiner respectfully disagrees. Firstly, the preamble of claim states system for *modeling* a bidirectional signal, and *not simulating*. As shown above Hsieh '800 teaches that the modeling is done with an FPGA forming a system. Further, Huang'593 is relied upon to provide this teaching. Further, In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicant's argument is considered and is found to be unpersuasive.

9. **Claims 3,8 & 16-17 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hsieh '800 in view of Mizoue'445.**

10. **Claims 9-10, 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsieh '800 in view of Mizoue'445, further in view of Huang '593.**

Regarding Claim 3, 8-10 and 13-17

Applicant has argued Mizoue'445 fails to remedy the teachings of Hsieh '800 and Huang'593. As stated above, *Hsieh '800 clearly teaches a system for modeling. Further, Mizoue'445 teaches simulation which complements the modeling performed by Hsieh'800 on FPGA.* It is known in art of modeling on FPGA that a software model of the circuit must be made before downloading it to be modeled on a FPGA. A simulation of such a circuit before modeling on FPGA is beneficial as it saves time and effort in case there are errors.

Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a

reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). It is known to one of ordinary skill in the art of modeling using a FPGA, that a software simulation model of the intended circuit is necessary to program the FPGA. In this case Hsieh '800 teaches use of FPGA to model interconnect with input/output (bidirectional) flow (Hsieh '800: Col.1 Lines 25-37). Mizoue'445 reference teaches simulating method for simulating a logic circuit (Mizoue'445: Col.1 Lines 9-17) such as the one modeled in Hsieh '800 reference.

Applicant further argues that there is nothing in Mizoue'445 that teaches switch level simulator that works for bi-directional switches. Examiner agrees and apologizes for the typo in the motivation. *Mizoue'445 reference is primarily used for simulation and storing the simulation results (Abstract).* Mizoue'445 presents no evidence that Mizoue'445 cannot model circuit described in the Hsieh'800 reference.

To clarify, the motivation to combine Mizoue'445 with Hsieh'800 would be that interconnect modeling system described in the Hsieh'800 is modeled on an FPGA and as known in the art for modeling on FPGA, storage is limited on such a FPGA based modeling system. Mizoue'445 is also concerned with size of simulation and writes the input and out to a file. Using the interconnect (bidirectional) model of Hsieh'800 with limited storage, simulation would require more simulation storage leading to the problem described in the Mizoue'445 (Mizoue'445: Background). This problem is remedied by Mizoue'445 thereby solving the problem of modeling and capturing the input/intermediate/output state problem in Hsieh '800 model by modeling it through his simulator/methodology. *Mizoue'445 teaches simulation which*

complements the modeling performed by Hsieh'800 on FPGA. It is known in art of modeling on FPGA that a software model of the circuit must be made before downloading it to be modeled on a FPGA. A simulation of such a circuit before modeling on FPGA is beneficial as it saves time and effort in case there are errors.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 9:30 - 6:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Monday, May 15, 2006

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